

REMARKS

Upon entry of the foregoing amendment, Claims 1-4, 7-9 and 14-16 are pending in this application. The Examiner rejected Claims 1-9 under 35 U.S.C. §102(b). Claims 1 and 7 have been amended, Claims 5-6 and 10-13 have been cancelled, and Claims 14-16 have been added in the foregoing amendment.

**Yanagisawa Does Not Anticipate
the Invention of Claims 1-4, 7-9 and 14-16**

Claims 1-9 were rejected under 35 U.S.C. 102(b) as anticipated by JP58-085572 ("Yanagisawa"). This rejection is traversed for the reasons discussed below.

Claim 1

Amended Claim 1 requires a first concavity in the bottom surface of the second semiconductor region and that a part of the first main electrode layer is buried in the first concavity. According to this configuration, the effective contact area of the first main electrode layer can be obtained by adjusting the depth of the first concavity. See page 23, lines 19-31 of the specification and Fig. 4.

The Examiner alleged that Yanagisawa describes the first main electrode layer being in contact with the second semiconductor region through a first concavity formed at the bottom surface of the second semiconductor region and cited the reference number 21 in Fig. 2G of Yanagisawa. As shown in Fig. 2G and Fig. 4 of Yanagisawa, the substrate 12 does not have any concavity. The electrode layer 21 is simply in contact with the bottom of the substrate. Thus, Yanagisawa does not describe a concavity cut into a semiconductor region or part of an electrode layer buried in the concavity, as required by Claim 1.

Accordingly, amended Claim 1 is not anticipated by Yanagisawa.

Claim 7

Claim 7 requires a via hole in the second semiconductor region and that a part of the first main electrode layer is buried in the via hole penetrating through the second

semiconductor region, configured such that the buried part of the first main electrode layer contacts with the first semiconductor region. According to this configuration, the first main electrode layer can contact the first semiconductor region 14 directly, providing low resistance. See page 24, line 8 to page 25, line 9 of the specification and Fig. 5.

The Examiner alleged that Yanagisawa describes a first main electrode layer, a part of the first main electrode layer being buried in a via hole penetrating through the second semiconductor region, configured such that the buried part of the first main electrode layer contacts with the first semiconductor region and cited the reference number 21 in Fig. 2G of Yanagisawa. As shown in Fig. 2G and Fig. 4 of Yanagisawa, the substrate 12 does not have any via hole. The electrode layer 21 is simply in contact with the bottom of the substrate. Thus, Yanagisawa does not describe a via hole in the second semiconductor region or part of an electrode layer buried in the via hole, as required by Claim 7.

Accordingly, amended Claim 7 is not anticipated by Yanagisawa.

Claim 14

Claim 14 requires that a concavity is cut at the top surface of the third semiconductor region, and that an ohmic contact electrode contacts the top surface of the third semiconductor region, a part of the ohmic contact electrode being buried in the concavity.

In contrast, as shown in Fig. 2G and Fig. 4 of Yanagisawa, the p⁺ type diffused surface region 18 of Yanagisawa does not have any concavity. The electric layer 20 is simply formed where a portion of the surface protection film 19 is removed. Thus, Yanagisawa does not describe a concavity cut into a semiconductor region or part of an electrode layer buried in the concavity, as required by Claim 14.

Accordingly, Claim 14 also is not anticipated by Yanagisawa.

Claim 15

Claim 15 requires that the first and second pn junction interfaces establish a single flat pn junction interface. Claim 15 also requires that the outer surfaces of the second, third and

fourth semiconductor regions establish a common chip outer surface of the semiconductor device and the chip outer surface is substantially orthogonal with the lower end surface of the first semiconductor region, and that a termination of the second pn junction interface is exposed at the chip outer surface.

In contrast, the p+ type diffused surface region 18 of Yanagisawa extends on only a portion of the n- type semiconductor layer 13. Although the p+ type diffused surface region 18 extends over the n type diffused surface region 16, Yanagisawa does not describe a single flat pn junction interface because the p+ type diffused surface region 18 does not extend over the entire n-type semiconductor layer 13. In Yanagisawa, only the outer surfaces of the substrate 12 and the layer 13 are exposed at the outer surface of the semiconductor device that is substantially orthogonal with the lower end surface of the layer 13. The termination of the pn junction interface of the p+ type diffused surface region 18 and the n- type semiconductor layer 13 is not exposed at the chip outer surface. See Fig. 2G and Fig. 4.

Accordingly, Claim 15 also is not anticipated by Yanagisawa and Claim 15 should be allowed.

Claims 2-4, 7-9 and 16

Claims 2-4, 7-9 and 16 depend either directly or indirectly from Claim 1 or 15. The remarks made above in support of the patentability of independent Claims 1 and 15 are equally applicable in distinguishing dependent Claims 2-4, 7-9 and 16 from Yanagisawa. Accordingly, Claims 2-4, 7-9 and 16 also should be allowed.

CONCLUSION

The foregoing is submitted as a complete response to the Office Action identified above. This application should now be in condition for allowance, and the Applicant solicits a notice to that effect. If there are any issues that can be addressed via telephone, the Examiner is asked to contact the undersigned at 404.685.6799.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Brenda O. Holmes", with a stylized, flowing script.

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